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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/847,620	05/02/2001	Jong-Kon Choi	9903-14	5622

7590 11/19/2002  
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EXAMINER

MITCHELL, JAMES M

ART UNIT PAPER NUMBER

2827

DATE MAILED: 11/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/847,620

Applicant(s)

JONG-KON CHOI

Examiner

James Mitchell

Art Unit

2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 09 August 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-13 and 16-18 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-13 and 16-18 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

**DETAILED ACTION**

***Allowable Subject Matter***

The indicated allowability of claim 13 is withdrawn in view of the new rejection.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 13 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 13 recites the limitation "the bonding wires" in Line 2. There is insufficient antecedent basis for this limitation in the claim.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by applicant's admitted prior art (APA).

The admitted prior art (Fig 1-3; Page 8, Lines 7-29) discloses a method for manufacturing a semiconductor DMD package comprising a wafer (Fig 3, step 71) including a plurality of DMD chips (12) with a plurality of mirrors (16) and a plurality of pads formed at the periphery forming a photoresist on a mirror (Page 2, Lines 14-16),

singulating a chip (steps 72 and 75) wherein the singulating comprises "fully cutting" the wafer (via half of the wafer fully cut), mounting the chip on top of a base substrate (20; step 77) and electrically interconnecting the bond pads (step 79), and removing the photoresist from the chip (73) and said package hermetically sealed (Page 1, Line 33).

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1, 2 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Thomas (U.S. 2002/0163055).

Thomas (Fig 1A-8;) discloses a method for manufacturing a semiconductor package, said method comprising: providing a wafer (102) including one or more chips, each chip having a one or more mirrors (103; Par. 0037) formed thereon and a plurality of electrode bond pads (106) formed on a periphery of the chip, forming a photoresist (107; Par. 0041, Line 5) over one or more of the mirrors, singulating one or more chip form (302; Par. 0050, Lines 5-6) by fully cutting wafer, mounting the one or more chip on a top surface of a base substrate (Fig 6), electrically interconnecting the bond pads of the chip to the base (505) via solder balls that are soldered and which inherently form a metallic adhesive between the chip and said substrate, and removing the photoresist from the chip (Fig 7-8; Par. 0073, Lines 4-5); further comprising inherently sealing (Par. 0080) the chip on an upper surface of the base substrate.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (APA) in combination with Mutsuo (JP 02-039442).

APA does not appear to show a metallic layer over the back surface of the wafer or a metallic adhesive, however Mutsuo (Fig 1) utilizes a metal layer (1) attached to the back surface of the semiconductor wafer with a metallic adhesive ("solder material"; Abstract).

It would have been obvious to one of ordinary skill in the art to incorporate a metal layer on the rear surface of the admitted prior art's wafer with a solder adhesive, in order to avoid defective bonding as taught by Matsuo (Abstract Purpose).

Claims 5, 6, 8 and 10-12, are rejected under 35 U.S.C. 103(a) as being unpatentable over APA as applied to claim 5 and further in view of Takehara (JP 356115548).

The APA further discloses (Fig 3) removing the photoresist from the semiconductor chips (step 73) and forming an anti-sticking film on the active surface of the chip (step 74), hermetically sealing said chip by forming a metal ring on the periphery of the base (Page 1, Lines 30-33), attaching a window lid to the upper surface of the ring (page 2, Lines 1-2), wherein a distance between the upper base substrate

and the lower surface of the lid is greater than the height of one or more bonding wires (as shown in Fig 2), a reflectance coating formed on the lower surface of the window (Page 2, Lines 2-3) and a moisture getter attached to the metal lid frame (Page 2, Lines 4-5) with a heat sink stud (60) to the lower surface of the base substrate.

APA does not disclose a low melting point metal layer consisting of lead on the back surface of a wafer, however Takehara teaches a method of forming a lapping metal layer consisting of lead on the back surface of a wafer (Abstract Constitution).

It would have been obvious to one of ordinary skill in the art to form a low melting point metal layer on the back of the admitted prior art's wafer in order to eliminate the improper connection of chips as taught by Takehara (Abstract Purpose). As such since the metal layer is placed over and covering a part of the wafer, it is lapping the back surface of the wafer.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over APA and Takehara as applied to claim 5 and further in view of Poradish et al. (U.S 5,293,511).

The admitted prior art does not appear to disclose that the base is ceramic, however Poradish utilizes a ceramic base.

It would have been obvious to one of ordinary skill in the art to form the base of the admitted prior art and Takehara with ceramic to support the device as taught by Poradish (Abstract).

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art and Takehara as applied to claim 5 and further in view of Shoji (JP 401053795).

Neither APA nor Takehara appear to disclose a method of forming a metallic adhesive, however Shoji teaches the use of a metallic adhesive.

It would have been obvious to one of ordinary skill in the art to modify the combined DMD structure of APA and Takehara by forming a metallic adhesive between the base and chip to improve joint strength as taught by Shoji (Abstract).

Claim 3, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thomas as applied to claim 1 and 16 and further in combination with Mutsuo (JP 02-039442).

Thomas does not appear to show a metallic layer over the back surface of the wafer or a metallic adhesive, however Mutsuo (Fig 1) utilizes a metal layer (1) attached to the back surface of the semiconductor wafer with a metallic adhesive ("solder material"; Abstract).

It would have been obvious to one of ordinary skill in the art to incorporate a metal layer on the rear surface of the Thomas's wafer with a solder adhesive, in order to avoid defective bonding as taught by Matsuo (Abstract Purpose).

### ***Response to Arguments***

Applicant's arguments with respect to claim 1-13 have been considered but are moot in view of the new ground(s) of rejection. Applicant noted that APA's step 80 did not contain the removal of a photoresist. Assuming that position to be true, applicant's step 73 is provided to establish removing a photoresist since it explicitly states removing a photoresist. Furthermore, since the claim language does not specify any specific sequence in its method, APA (Fig 3) reads on the "comprising" language.

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Art Unit: 2827

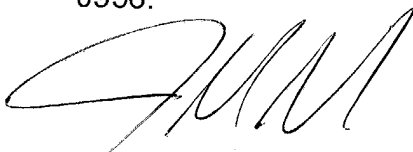
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**Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Mitchell whose telephone number is (703) 305-0244. The examiner can normally be reached on M-F 10:30-8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3230 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

  
jmm  
November 17, 2002

  
ALBERT W. PALADINI  
PRIMARY EXAMINER